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This paper investigates the low-frequency noise properties of multilayer WSe_2 field effect transistors (FETs) in subthreshold, linear, and saturation regime. The measured noise power spectral density of drain current (S_{ID}) shows that the low-frequency noise in multilayer WSe_2 FET fits well to a $1/f^{\gamma}$ power law with $\gamma \sim 1$ in the frequency range of 10 Hz–200 Hz. From the dependence of S_{ID} on the drain current, carrier mobility fluctuation is considered as a dominant low frequency noise mechanism from all operation regimes in multilayer WSe_2 FET. Extracted Hooge's parameter in this study is within the value of 0.12, comparable to those of the transition metal dichalcogenide FETs in recent reports. © *2015 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4906141]

Recently, ultra-thin films of transition metal dichalcogenides (TMDCs)[1] have been actively studied for the alternative opportunities to serve as two dimensional (2D) active layers beyond graphene. Particularly, TMDCs, which have intrinsic band gaps,[2,3] are very attractive for the envisioned nano-electronic applications due to its unique electrical,[4,5] chemical,[6,7] and optical properties.[8] Among various TMDC layers, predominant research activities have been noticeably toward single and/or multi-layer MoS_2 field effect transistors (FETs) with typical n-type characteristics associated with relatively easy preparation of thin films via exfoliation and/or chemical vapor deposition (CVD),[9,10] compared with other candidates in TMDCs. However, WSe_2 FETs with typical p-type properties can be very appealing for the applications of nanoscale complementary circuits and switching backplanes for flat panel display (FPD) due to their high mobility (~100 $cm^2/V{\cdot}s$), excellent on/off ratio(~10^7), and low sub threshold swing (SS, ~70 mV/decade).[11,12] Meanwhile, for the aforementioned applications based on TMDCs, their device stability, and flicker noise characteristics should be carefully investigated because of their inherent structures of 2D van der Waals materials with a large surface-to-volume ratio, which are easily prone to physical adsorption and/or chemisorption of surface contaminants on TMDCs.[6,7] Nevertheless, research activities, especially for low-frequency noise (LFN) properties which can be one of key aspects for the "all-surface" structure of 2D materials,[13,14] have been rarely reported for WSe_2 FETs as one of promising p-type candidates in TMDCs, whereas low frequency noise characteristics for typical n-type MoS_2 FETs have been actively researched.[15–17]

Here, we report multilayer WSe_2 FETs encapsulated with a hydrophobic polymer (CYTOP) which allows to operate stably in air.[18,19] Furthermore, the LFN characteristics of WSe_2 FETs in air are reported in all operation regimes (i.e., linear, sub-threshold, and saturation regime).

Fig. 1(a) shows the perspective view of a multilayer WSe_2 FET with a bottom gate structure. An n-type silicon wafer with heavy phosphorus doping ($\rho \sim 0.005\ \Omega{\cdot}cm$) was used as a starting substrate, which also plays a role as back gate electrodes. After thermal oxidation in dry oxygen at 950 °C, 10 nm thick thermal oxide was grown on the heavily doped Si wafer and serves as gate insulator. Photoresist (PR) patterning for lift off and Cr deposition (~50 nm) are followed by PR removal to form alignment marks on each sample. WSe_2 flakes were mechanically exfoliated from bulk WSe_2 crystals by using polydimethylsiloxane stamps and immediately transferred onto the SiO_2/Si substrate. The multi-layer WSe_2 flakes on the substrate were annealed at 350 °C for 2 h in the ambient of a mixed gas of argon and hydrogen. Photolithographic pattering and electron-beam evaporation of Pd (~50 nm), followed by lift-off in acetone, creates source and drain electrodes on WSe_2 with good Ohmic contact.[6] After forming S/D electrodes on WSe_2 flakes, layer thickness for each device was measured by atomic force microscopy (AFM), as shown in Fig. 1(b). The thickness of a multi-layer WSe_2 flake measured by the AFM is 27 nm which approximately corresponds to 40 layers. Finally, the backside of the WSe_2 flake was encapsulated by fluorinated polymer (CYTOP; CTL-809M, Asahi Glass Co., Ltd.) with typical spin coating process. After thermal evaporation of SiO_x (~50 nm) on the CYTOP, for a surface promoter layer during PR coating, pad opening was completed by dry etching ($\sim O_2/CF_4$) via PR patterns.

Fig. 2(a) shows the transfer characteristics of a fabricated multilayer WSe_2 FET with a ratio of width to length ($W/L = 30/10\ \mu m$) at a drain-to-source voltage (V_{DS}) of −0.1 V. The electrical characteristics of the devices were measured by using a precision semiconductor parameter analyzer (Agilent B1500A). The curves show typically observed p-type behaviors with a sub-threshold slope (S) of 120 mV/decade, a field effect mobility (μ_{FE}) of 80 $cm^2/V{\cdot}s$, a threshold voltage (V_{th}) of −0.7 V, and an on/off ratio of ~10^6, where V_{th} was calculated by fitting a straight line to the measured transfer curve. The field effect mobility was

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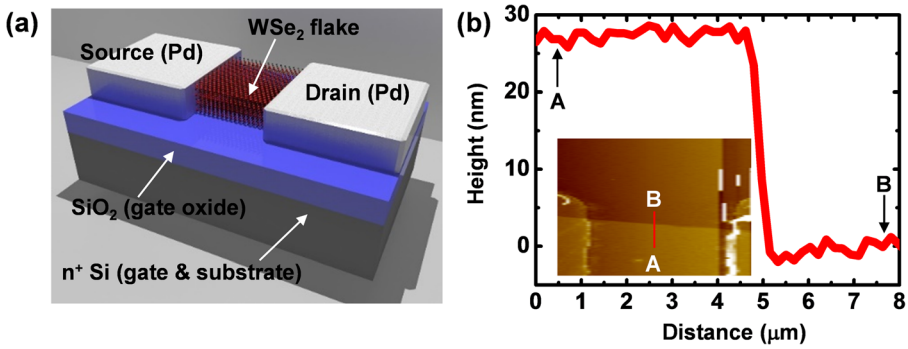

FIG. 1. (a) A schematic diagram for multi-layer WSe_2 FETs with Pd contact. (b) Height profile for a multilayer in the channel of representative WSe_2 FETs, which has been scanned along the red line from A to B in the channel by atomic force microscope. The inset in Fig. 1(b) shows the AFM images for the channel regime for WSe_2 FETs. The channel length and width is 10 μm and 30 μm, respectively.

extracted from maximum point of transconductance ($g_{m\_max} \sim 8.64\ \mu S$) according to

$$\mu_{eff} = \frac{Lg_m}{WC_iV_{DS}}, \quad (1)$$

where C_i and g_m are the gate capacitance per unit area and the transconductance, respectively. Fig. 2(b) shows the output curves for the fabricated WSe_2 FET, which exhibits a clear current saturation and pinch-off behavior. In addition, current crowding around low drain bias (~ -0.1 V) was not observed, which indicates that good Ohmic contacts between WSe_2 and Pd were formed.

Fig. 3(a) shows the S_{ID} of the device measured in the sub-threshold, linear, and saturation regimes by using low-noise current preamplifier (SR570) and dynamic signal analyzer (Agilent 35670A). Measured S_{ID} nicely follows the behavior of $1/f^{\gamma}$, where the γ is close to 1 in the frequency less than $\sim$200 Hz in all operation regimes. Historically, two different mechanisms[20] have been considered to explain the 1/f noise in metal-oxide-semiconductors (MOSs) FETs associated with fluctuations in carrier mobility (Hooge[21]) or carrier number (McWhorter[22]). Carrier mobility fluctuation is mainly caused by lattice scattering of carrier,[21] whereas carrier number fluctuation is predominately attributed to the number of carrier fluctuating due to trapping-detrapping process.[22]

One of methods to distinguish the origin of fluctuations coming from carrier mobility (or carrier number) in FETs is to analyze the S_{ID} of the drain current under gate and drain bias condition. In sub-threshold and linear regime, the drain bias was fixed at -0.1 V and the gate bias was changed from -0.03 V to -1.4 V. Fig. 3(b) shows that the S_{ID} versus drain current has a linear relationship from sub-threshold to linear

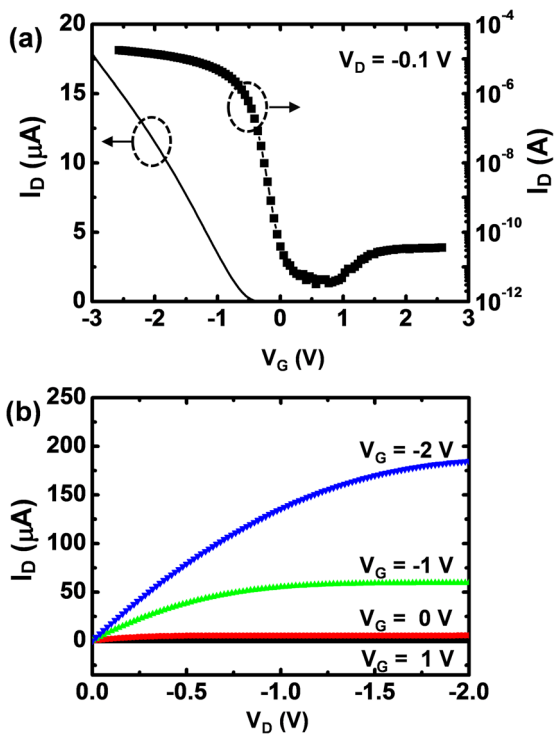

FIG. 2. (a) Transfer characteristics for multilayer WSe_2 FETs with CYTOP passivation measured in the linear operation regime at the drain bias of $V_{DS} = -0.1$ V. (b) Output characteristics for the same device correspond to gate bias values from 1 V to -2 V, with -1 V step, for the drain bias (V_{DS}) from 0 V to -2 V.

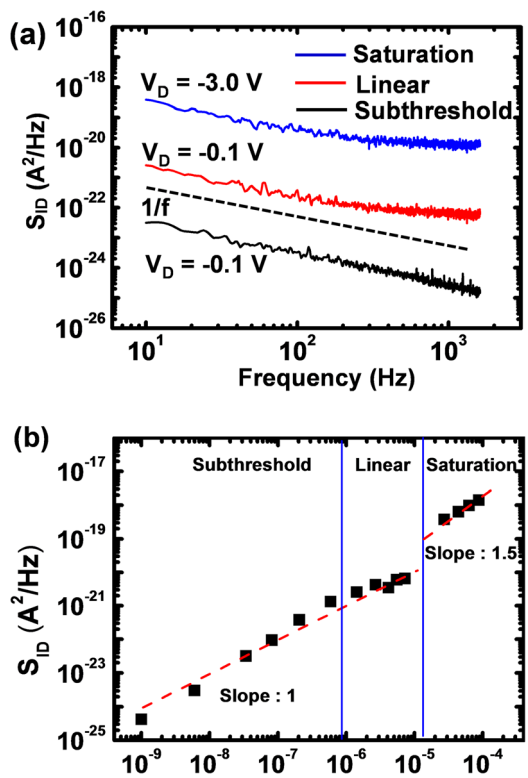

FIG. 3. (a) Drain-current noise spectral densities S_{ID}'s for the device which were measured at different operation regimes, respectively, sub-threshold ($V_{GS} = -0.03$ V and $V_{DS} = -0.1$ V), linear ($V_{GS} = -0.8$ V and $V_{DS} = -0.1$ V), and saturation regimes ($V_{GS} = -1$ V and $V_{DS} = -3$ V). (b) Measured noise power spectral densities (S_{ID}) vs drain current (I_D) at a fixed frequency of 10 Hz. The bulk mobility fluctuation was observed in all operation regimes. Line and dotted-line curves correspond to experimentally measured and theoretically estimated data, respectively.

regime, which substantiates that the low frequency noise is mainly coming from the carrier mobility fluctuation. From Hooge's empirical law, the S_{ID} can be expressed as[23]

$$S_{ID} = \frac{q\mu_{eff}}{L^2}\frac{\alpha_H}{f} I_{DS} V_{DS}, \quad (2)$$

where f is the frequency, q is the elementary electron charge, and α_H is Hooge's parameter that is subjected to compare the noise level in different devices and materials. Furthermore, Fig. 3(b) shows that the S_{ID}, measured in the saturation regime, is approximately proportional to the 3/2 order of I_D. The result hints that mechanism of low frequency noise in the saturation regime is also coming from carrier mobility fluctuation. In the saturation regime, Hooge's empirical relation can be expressed as[24]

$$S_{ID} = \frac{\alpha_H}{f} q\sqrt{2}\frac{\mu_{eff}^{1/2}}{C_i^{1/2} W^{1/2} L^{3/2}} I_{DS}^{3/2}. \quad (3)$$

Low frequency noise characteristics for WSe_2 FETs in this study show that the behavior of flicker noise consistently obeys the Hooge's empirical laws (i.e., carrier mobility fluctuation) in all operation regime (linear, sub-threshold, and saturation regime). This implies that the influence of traps nearby the interface between gate dielectric ($\sim SiO_2$) and multi-layers of WSe_2 is significantly weak in the transport of the channel carriers, which might be related with the accumulated channel charge distribution deeply located from the interface.[5] The origin of the distribution is probably associated with a long Thomas-Fermi charge screening length ($\sim$7 nm), possibly observed for van der Waals layered WSe_2, which has been reported for MoS_2 FETs with multi-layers ($\sim$40 nm).[25] In addition, encapsulation of CYTOP can lead to the reduction of chance for carrier number fluctuation possibly caused by physical and/or chemical adsorbates on the channel of WSe_2 FETs.[25] Furthermore, the potential barrier between the multi-layer WSe_2 and the gate insulator (SiO_2), probably formed by van der Waals forces, might be one of possible reasons for weak influence from interface traps.[17]

Fig. 4 shows several Hooge's parameters for FETs with TMDC channel layers, which have been reported in the literature.[26,27] All parameters were extracted from the linear regime. The square symbols in Fig. 4 indicate the values of Hooge's parameters for FETs with MoS_2 channel layers synthesized by CVD.[26] The extracted values (for square symbols) were estimated from the low frequency noise characteristics of MoS_2 FETs measured in air ambient. Both circle and up-triangle symbols represent Hooge's parameters extracted from FETs with exfoliated MoS_2 layers and the parameters were measured either in vacuum or air.[27] The value for down-triangle in Fig. 4 was extracted from WSe_2 FET in this work. The Hooge's parameter for WSe_2 FETs in this study is about 0.12, which is similar to (or slightly larger than) those of exfoliated MoS_2 FETs (or CVD MoS_2 FETs).

In summary, we have investigated low frequency noise characteristics of a FET with multi-layer ($\sim$27 nm) WSe_2 as a channel material. This device showed a good Ohmic contact behavior and stable operation in air by adopting hydrophobic CYTOP layer as an encapsulation layer. In all

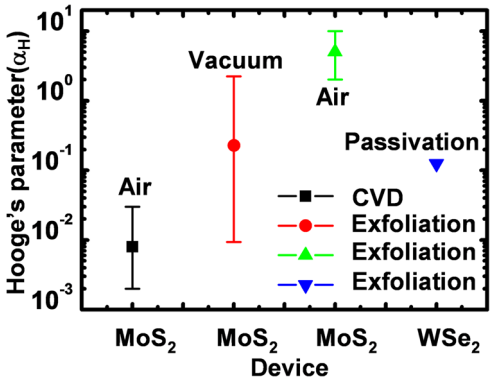

FIG. 4. Extracted Hooge's parameters for MoS_2 and WSe_2 FETs, which have been reported in the literatures. Each symbol for square (■), circle (●), and up-triangle (▲) corresponds to MoS_2 FETs. However, fabrication method, number of flakes, and measurement environments were not exactly the same. The down-triangle (▼) indicates the data for WSe_2 FET in this experiment.

operation regime, the low frequency noise characteristics of the WSe_2 FET obey consistently Hooge's empirical relation, which indicates mobility fluctuation is a dominant mechanism responsible for the drain current fluctuation. These results might be attributed to weak interaction between the accumulated holes in the channel and the traps at the interface since the channel carriers in the WSe_2 are away from the interface. Extracted Hooge's parameter in this work is within the value comparable to those of the TMDC FETs in recently published literatures.

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